Design Automation Technical Committee
DATC

IEEE COMPUTER SOCIETY

ELECTRONIC DESIGN PROCESSES (EDP) 2008 – CALL FOR PAPERS

APRIL 17-18th, 2008

MONTEREY BEACH HOTEL, MONTEREY, CALIFORNIA

The Electronic Design Processes (EDP) Workshop provides a forum for a cross-section of the design community to discuss state-of-the-art electronic design processes and CAD methodologies. The workshop focuses on the improvement of the overall design process, rather than on the functions of the individual tools themselves. Please visit http://www.eda.org/edps to see the list of past EDP Workshop speakers and presentations: 2007, 2006, 2005, 2004, 2003, 2002, 2001, 2000.
Here is a printable version of this CFP: http://www.eda.org/edps/edp08/edp08-cfp.pdf

Registration and Hotel:

Please make hotel reservations with the Monterey Beach Resort directly; the IEEE/EDP rate provides Gardenside rooms for $119 single/double, and Oceanside for $169 single/double. **Please mention the code EDP4/16/08 when booking your room**. Space at the hotel is limited, and rooms must be reserved by March 17 to guarantee space and the reduced rate. On-line registration for the workshop will be available shortly.

THEMES IN 2008: Portable Devices, Design for Manufacturing

We solicit papers and proposals for special/panel sessions that shed light on the methodologies used for real current and future chip and system designs. Topics include but are not limited to:

- Methodology for the rapid design of embedded/portable systems
- Best practices and experiences with Power or DFM Methodology focus
- Multi-voltage Design and Power Management, Power Analysis
- Restrictive Design Rules (RDR) Impact on DFM
- Process/Device Characterization, Modeling implications
- Standards Activity: Helping or Hurting?
- Status of EDA Industry
- Multi-Core Programming/Implications
- Flow Integration, Scaling, and Migration
- Human Issues: Large & Distributed Teams, Off-shoring, Training and Education
- Key Trends: Future Methodology Needs, Impact of Design Manufacturing Interface, Interoperability, Impact of Web, Licensing Models, and Platform

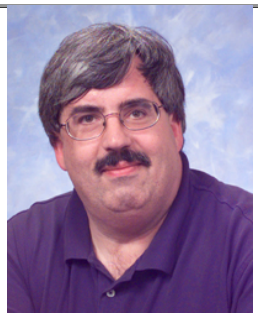
PAPER SUBMISSION

Authors should submit full-length, *original and unpublished* papers (maximum 20 pages in single-column double spaced format, or 6 pages in double-column conference proceedings format) along with author contact information. Proposals for special and panel sessions may also be submitted; a 1-page description along with organizer contact information is required. Send Proposals via email to: edps@eda.org

IMPORTANT DATES

Submission Deadline: 29 February 2008 **Acceptance Notification:** 17 March 2008
Camera Ready Copy: 31 March 2007 **On-site Registration:** 16 April 2007

EDPS 2008 Preliminary Workshop Program:

Speaker	Affiliation	Title/Area of Talk
Wednesday, April 16, 2008		
Registration		
05:30-7:00 PM Evening Reception @ Captain's Table		
Thursday, April 17, 2008		
08:30 AM - 09:10 AM Welcome  Host: Patrick Madden, SUNY		
Keynote Address **Timothy G. Mattson / Intel** **Parallel Computing: Can We Please Do it Right?**		
Session: Embedded Microprocessor Design Session Chair: TBD		
Grant Martin, Steve Leibson	Tensilica	 Embedded Boot Camp: AMP vs. SMP
Radhika Thekkath	MIPS	Max Out Your Multi's
Ian Rickards	ARM	
Ray Brinks	Sonics Inc	Microprocessor Centric SoC's are

Ray Brinks	Sonics Inc.	Dead
Session: EDA Standards Panel Session Chair and Organizer: John Darringer (IBM)		
John Darringer	IBM	
Gary Delp, Technical Director	SPIRIT	
Jake Buurma and Steve Schulz, President	SI2	
Victor Berman, Chairman	IEEE DASC	
Rohit Kapur, Chairman	IEEE TTSC	
Session: Manufacturing Challenges and Solutions Session Organizer: TBD		
Puneet Gupta	UCLA/Blaze	
Andres Torres	Mentor Graphics	 Regular Designs and Computational Lithography: Their Past, Present, and Future

Bhanu Kapoor, Auturo Salz, Shankar Hemmady	Mimasic/Synopsys	Multi-Voltage Power Managment Verification Issues
Srivasta Vasudevan	Synopsys	Verification Minimization with Karnaugh Maps
Session: Nuts and Bolts of EDA Tools Session Chair: TBD		
Patrick Groeneveld	Magma	 TCL as an EDA tool flow integrator: the good, the bad, and the ugly.
Joao Gaeda	CLKda	 Efficient Use of Multicore Processors for Timing Analysis
Igor Markov	U Michigan	 On Libraries, Reuse, and the Value of EDA Software

EDP Banquet Dinner

Friday, April 18, 2008

Session: EDA Venture Capital Outlook

Juan-Antonio Carballo	Argon VC	

Session: Standardization and Virtualization

Aman Joshi	Director of IC Tools, Sun Microsystems	OpenSparc
Larry Lapides	Imperas	Open Virtual Platforms
Michel Genard	Virtutech	Virtualized Software Development

Sessions: ESL and High Level Design

Session Organizer: TBD

Rajesh Gupta	UC San Diego	 The Next EDP Challenge: Cost of ASIC Design & Validation
Rishiyur Nikil	Bluespec	
Alec Stanclescu	FinTronic	

Session: Renewing and Educating on IEEE on Design Standards Processes

Session Organizer: Alec Zamfirescu

TBD		

Closing Remarks

Organizing Committee:
General Chair: Patrick H. Madden
Technical Program Chair: Gary Smith
Steering Committee Chair: Bhanu Kapoor
Publicity Chair: Steve Grout

Program Committtee:

Michael Bohm (AccelChip) **Aparna Dey (Cadence)** **John Lillis (UIC)**
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Bhanu Kapoor (Mimasic) **Patrick Madden (Binghamton)** **Dennis Sylvester (U. of Michigan)**
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Steve Grout (Consultant) **Dwight Hill (Synopsys)** **Patrick Groeneveld (Magma)**