

Test Technology Newsletter

July - September, 1999



The Newsletter of the Test Technology Technical Council
of the IEEE Computer Society



Chair's Message

The last three months we saw a list of very successful TTTC sponsored events, such as VTS, Signal Propagation Workshop, South West Test Workshop, European Test Workshop, TECS, and IOLT Workshop, to name few. Some of these events are reported on in this issue. Now, most of us are concentrating on our individual preparations for ITC/Test Week, either by finalizing our company exhibits, preparing our PowerPoint files for our ITC paper, or putting the final touches on our workshop presentation. TTTC also is going through a similar busy period to be prepared for ITC/Test Week. ITC is the premiere test event of the year. The exhibition floor of ITC brings together the state-of-the-art in test products, while the conference sessions compete over the audience to present attractive test solutions. TTTC not only cosponsors this premiere event, but it also augments it with several other attractive units to make Test Week the most complete offering to the test community. These augmented units, which

(Continued on page 2)

The 30th International Test Conference (ITC 99)

The 1999 International Test Conference celebrates its 30th year. The premier conference for test technology, and sponsored by TTTC, ITC continues its well established format for Test Week with two days of tutorials and a three day conference program followed by two days of workshops. This total package has been put together with the theme of "Test and the Product Life Cycle" very much in mind.

For the Plenary this year we have presentations from Patrick Gelsinger, VP of Intel (Keynote Speaker) who will present "The Challenges of Design and Test for the World Wide Web." Jeevan Perera, Research Fellow at NASA's Johnson Space Center and our Invited Speaker, will talk about Reliability Modeling for Microelectromechanical Systems, continuing ITC's coverage of the interesting MEMS area.

In addition to ITC's coverage of interesting and high quality materials, including design for diagnostics, microprocessor test, production testing, ATE, test synthesis and test generation/fault simulation, there are the sessions and presentations supporting the Conference theme "Test and the Product Life Cycle". Time-to-Market matters will be directly addressed to explore how DFT affects it and other more tangible variables; the effects of chip-level DFT on board test, and the added complexities of system test will be discussed.

Don't forget the unforgettable panels! The first day evening panels are preceded by complimentary food in the exhibits hall - giving you added energy for discussion!

ITC Test Week does not end there. A now regular feature of Test Week includes workshops - separate events dedicated to particular topics. The workshops (Production Test Automation, Microprocessor Test and Verification, and System Test and Diagnostics) continue from after the panels through the next day. These are excellent events to discuss your chosen field.

In short, make sure you get a copy of the Advance Program, book early for registration discounts (and confirm your copy of the hard copy proceedings!), and then we can look forward to seeing you in Atlantic City in September.

Tony Ambler, ITC 99 Program Chair



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comprise TTTC's additional contribution to Test Week, include: the Test Technology Education Program tutorials (see below); three leading-edge parallel workshops (see the ITC 99 article, front page); six working group meetings of test technology standards, an IEEE Design & Test Round Table sponsored by TTTC, an Awards Banquet to present the annual service awards winners, a TTTC information booth with ample data on upcoming activities, and numerous other fringe meetings for TTTC committees (see page 3). I am sure you will be participating in several of the above forums.

In the next two months, the TTTC Communications Group will make sure you are well informed about all the forums taking place at ITC/Test Week. The Communications Group is headed by Paolo Prinetto and, in addition to this Newsletter, it is comprised of TTTC's Electronic Broadcasting Medium, web site and its new initiatives, the Monthly Planner, TTTC Booths at Technical Events, embedded Newsletters in IEEE Design & Test and JETTA, and finally, the consolidated database (see page 7), which is the backbone of the Communications Group.

This Group and the rest of TTTC's operational model was a topic of discussion at the last IEEE Computer Society's Technical Activities Board (TAB) Meeting in June 99. I am pleased to inform you that the presentation I made and the discussions that followed were extremely well received by TAB. Our structure, activity domains and operation are being looked at as models for many active TC's. Thanks to your efforts and contributions TTTC holds an exemplary status today.

TTTC is a dynamic organization and can grow or shrink depending on the needs of our test community. I am pleased to let you know that in the last few months I have received an increasing number of offers from many of you to get involved in TTTC's ongoing and new activities. TTTC has a long way to go before it becomes the ideal organization that fully supports our test community with its professional needs beyond the actual organizations we work for. Hence, please feel free to jump in at any time and bring your own contribution in various available capacities. This summer, we will be electing officers for the next two-year term, 2000-2001. This includes the TTTC Chair and two Vice Chairs. As I get closer to completing my two term limit at the end of 1999, I feel that there are many more new areas that TTTC can expand and bring value to. I am sure the new Chair and Vice Chairs, while leveraging the recent TTTC successes, will build on them and expand them to such new areas.

I look forward to seeing you at ITC/Test Week and discussing with you this and other topics of common interest.

Yervant Zorian
Chair, Test Technology Technical Council



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ITC 99

TTTC TUTORIALS AT ITC 99

The TTTC Tutorials & Education Group has started a comprehensive Test Technology Educational Program (TTEP). Starting in 1999, this program provides opportunities for design and test professionals to update and expand their knowledge-base in test technology, and earn official certification from the IEEE TTTC, upon the completion of four full day tutorial units offered by TTEP. The Test Technology Educational Program schedule for 1999 includes tutorial units presented at the following TTTC-sponsored Technical Meetings:

- VLSI Test Symposium (VTS), Dana Point, CA, USA, April 25 and April 29.
- European Test Workshop (ETW), Constance, Germany, May 25.
- International Test Conference (ITC), Atlantic City, NJ, USA, September 26-27.
- DFT Symposium, Albuquerque, NM, USA, October 31.
- Asian Test Symposium (ATS), Shanghai, China, November 16

At ITC 99, TTTC is pleased to present sixteen full-day tutorials on topics of current interest to test professionals and researchers. Eight tutorials are held on Sunday, September 26th, and eight on Monday, September 27th.

SUNDAY, SEPTEMBER 26TH

1. System Diagnosis: Approaches for Modeling and Analysis
2. The Fundamentals of Digital Semiconductor Testing
3. Boundary Scan and Other 1149.x Standards
4. DFT Techniques: A Comparative Analysis
5. BIST Implementation and Applications - from Chip to System
6. Memory Testing: Fault Models, Algorithms, and Tests
7. Metrics, Techniques and New Developments in

- Mixed-Signal Testing
8. IDDQ Testing

MONDAY, SEPTEMBER 27TH

9. Functional Design Verification: Process and Methods
10. An Introduction to Successful Board-Test Strategies
11. Strategies for Implementing Functional Test Systems Using VXI and PXI
12. Built-In Self-Test for System-on-a-Chip
13. Test Strategies for High Density Packages
14. Embedded Memory Test
15. IC Techniques for Mixed-Signal DFT and BIST
16. New Validation and Test Problems for High Performance Deep Sub-micron VLSI Circuits

All tutorials qualify for credit towards IEEE TTTC certification under the TTEP program. Each tutorial requires a separate registration fee. Please see the ITC registration form or contact Courtesy Associates (202-331-2000) for further information.

Attendees of tutorials receive study material, handouts, breakfast, lunch, and two coffee breaks. The study material includes copies of the presentation and bibliographical material, and, when applicable, a relevant textbook (textbooks are provided to attendees who register at IEEE/CS member or non-member rates).

For more information on this program contact the Tutorials & Education Group Vice-Chair Anand Raghunathan (anand@ccrl.nj.nec.com).

If you are interested in presenting a tutorial as part of TTEP 2000, please contact Joan Figueras, Tutorials & Education Group Vice-Chair (figueras@eel.upc.es). A program committee will review the received proposals and develop an annual TTTC educational program.

Anand Raghunathan, Tutorials & Education Group Vice-Chair (anand@ccrl.nj.nec.com)



TTTC Workshops at ITC 99

Sunday, 26 September

4:30 pm - 7:00 pm ExCom
Contact: Y. Zorian, zorian@logicvision.com

Tuesday, 28 September

11:30 am – 1:00 pm European Group (ETTTC)
Contact: C. Landrault, landrault@lirimm.fr

5:30 pm – 7:00 pm Standards Group (TTSC)
Contact: P. McHugh, p.McHugh@ieee.org

Wednesday, 29 September

7:00 am – 9:00 am Meetings Group (TMRC)
Contact: D. Gizopoulos, dgizop@4plus.com

11:30 am – 1:00 pm Technical Activities Group
Contact: T. Ambler, ambler@ece.utexas.edu

5:30 pm – 7:00 pm Tutorials and Education Group
Contact: M. Nicolaidis, michael.nicolaidis@imag.fr

Thursday, 30 September

7:00 am – 9:00 am OpCom
Contact: Y. Zorian, zorian@logicvision.com

Please check at the registration desk at ITC 99 for any late changes in scheduling.

TTTC Technical Meetings

5th International Mixed-Signal Testing Workshop (IMSTW 99)

IMSTW 99 was held 15-18 June at the Delta Whistler Resort, in Whistler, British Columbia, Canada. The workshop was sponsored by the IEEE Computer Society TTTC, the University of British Columbia and several corporations. This year the workshop attracted 80 participants from industry and academia from 16 different countries. Close to half the participants were from Canada and the USA and about the same proportion from industry.

The program this year was organized by M. Renovell, LIRMM, France, and by M. Sachdev, University of Waterloo, Canada, and A. Ivanov, UBC, Canada. In his words of welcome, A. Ivanov suggested that this 5th version of the workshop could mark the field of mixed-signal testing as emerging out of "infancy" analogous to children formally entering school at that age. The program featured 31 papers organized in 10 Sessions on the following topics:

1. Test Generation and Testability Measures
2. Current-Based Testing
3. Virtual Test (2 sessions)
4. Applications of the 1149.4 Test Bus
5. New Developments in Test Techniques and Approaches
6. Fault Simulation and Extraction
7. BIST (2 sessions)
8. Fault Diagnosis and MEMS

The program also included 13 posters on various mixed-signal testing topics, one mini-tutorial on the 1149.4 Mixed-Signal Test Bus, and one Panel Session. The mini-tutorial by S. Sunter, LogicVision and Vice Chair of the 1149.4 Working Group, was very well received by the audience. The panel, organized by A. Richardson, Lancaster University, and M. Sachdev, University of Waterloo, was entitled: "Testing Systems on a Chip: Role of Mixed-Signal Test". It was scheduled for 1 1/2 hours but was so successful in generating discussion that it had to be interrupted for dinner after going on for more than 2 hours! Stay posted for the highlights of the discussion which will soon be reported in a TTTC sponsored publication.

Besides working and discussing mixed-signal test topics, participants had a chance to test their skills on surrounding Whistler mountain cycling trails during a "social event" session. This cycling test was followed by a Pacific Northwest theme evening that culminated in a "Klondike Gold Rush Casino" session with a final auction sale! Participants clearly fully enjoyed the "mixed-signal and t*sting" evening.

Next year the workshop will be in Montpellier, France, organized by M. Renovell and his colleagues at the LIRMM in Montpellier, and promising to be a very successful "vintage". The dates will be 21-23 June 2000. Please contact renovell@lirimm.fr for details.

André Ivanov, IMSTW 99 General Chair



ETW 99 Turns Out to be the European Test Event

More than 120 attendees discussed topics of test and testable design of microelectronic systems at the IEEE European Test Workshop (ETW 99) in Constance, Germany, end of May 1999. The workshop had a special track of sessions "Industrial Experiences and Challenges" during all the three days which received a lot of attention and caused lively discussions. This track laid special emphasis on test economics, test of core-based systems, testability support of processor cores and memory test. G. Francis from Philips (UK) discussed the efforts needed to reach a ppm quality level in consumer electronics and pointed out that the abstract stuck-at fault model is not sufficient any more and that more sophisticated defect analysis has to be done. D. Appello (STMicroelectronics, Italy) described economic criteria for test strategy selection and proposed software based BIST solutions. After both presentations, the difficulties in convincing the product management that efforts put into design for test and built-in self-test during the early design phases will really pay off during the product life cycle were mentioned. This short termed management view is still found in some companies while the real numbers which are reported even at this workshop emphasize the economic advantage of early test considerations.

The same large amount of attention was attracted by the description of the test features of processor cores. Pete Harrods (ARM Ltd. UK) described the test experiences with the widely used ARM processor core which has to support a variety of test strategies as it must fit into the user defined system test. Starting with the standardized boundary scan solution, more sophisticated core tests have to be compliant with new IEEE 1500 and VSI efforts for standardization. Both the ARM core and the TriMedia CPU64 presented by H. Vranken (Philips Research, NL) provide extended means for system debugging and emulation.

W. Daehn from Infineon (formerly Siemens Semiconductors) drew the attention to memory test problems. Since the capacity of memory chips increases much faster than their speed, test application times will be uneconomically long. This effect cannot be handled any more by exploiting parallelism and built-in self-test as power consumption and electromagnetic compatibility will set limits. Hence, in approximately two more generations, new memory chip architectures, organization, packages and test methods will be required.

Other sessions of the workshop were oriented towards basic research and had more presentations from academic institutions. Focal point of European microelectronics is systems engineering, including analog and mixed-signal modules, and testing and simulation of these parts were the topic of several discussions. Another theme was built-in self-test of digital systems under certain constraints: the BIST architecture should not be intrusive into the mission logic while increasing fault coverage, and the power and energy consumption during BIST should not exceed the system specification. For both cases, solutions were presented which generate precomputed deterministic patterns on chip and mask useless patterns which do not contribute to the fault coverage.

In over 50 presentations nearly all fields of testing

microelectronic systems were addressed as automatic test equipment, test generation, I_{DDQ} testing, and test of micro-electromechanical systems (MEMS). Both presentations and attendees came from approximately half from industry and half from academia. In his concluding remarks, the general chair of the workshop, Hans-Joachim Wunderlich, University of Stuttgart, made the observation that the basic research oriented sessions were very well attended by professionals from industry, perhaps with the expectation to find hints here for solving their practical problems. On the other hand, researchers and teachers were very interested in the more practical sessions in order to get information about real problems and topics for further research.

In conjunction with the workshop, professional organizations performed fringe meetings (SEMI and IEEE Test Technology Technical Council), and two full day tutorials were offered. Sandip Kundu and Sreejit Chakravarty from Intel Corporation, Santa Clara, talked about the test problems of nanometer technologies: a status update, and E.J. Marinissen (Philips) and Y. Zorian (LogicVision) taught about testing embedded-core based system chips. Both tutorials were well attended mainly by representatives from the local industry of the south of Germany. During one late afternoon and evening, a boat trip on Lake Constance, a visit of the Meersburg Castle, and a walk and dinner on the flower island Mainau gave excellent opportunities to the participants for discussions, establishing professional contacts and deepening personal relationships.

In a final review nearly all of the attendees claimed to enjoy the workshop, found it extremely useful under professional aspects and were highly satisfied with the organization. They plan to come again to the European Test Workshop in the year 2000, which will include tutorials and fringe meetings again. ETW2000 will be held nearby Lisbon, Portugal, and together with tutorials and fringe meetings it will be in the last week of May: the European Test Week 2000.

H.-J. Wunderlich, ETW 99 General Chair



8th IEEE North Atlantic Test Workshop (NATW 99)

The 8th Annual IEEE North Atlantic Test Workshop (NATW) was held at the Whispering Pines Conference Center at the University of Rhode Island on 27-28 May, 1999. The workshop again successfully attracted industry leaders and internationally recognized engineers to discuss current test issues and trends. The theme of the workshop was "Reliability and Testing Issues for the 21st Century."

Dr. Samuel H. Fuller delivered a keynote speech on "The Challenges of Testing Future Mixed Signal Products." Dr. Fuller, an IEEE Fellow, is currently the Vice President of R&D, Analog Devices Inc. The keynote speaker pointed out that the test cost to product cost ratio has been steadily increasing for analog and mixed signal products. In one example with a Teradyne tester, the test cost is already up to 25% and may soon go up as high as 50% of product cost. This year's workshop also included a panel session discussing "Manufacturing Systems on Silicon (SOC) Containing Mixed Signal Components." The panel was organized by James Monzel of IBM. The four panelists were: Bozena

Technical Activities

Formation of TAC for Virtual Test

Ed Perkins is heading up the effort to see if there is interest to support formation of a TAC for Virtual Test methodology in the TTTC. He is planning on holding an organizing meeting during ITC 99. Presently, there are several people interested in this fledgling activity and hopefully enough interest will be shown to form a critical mass to sustain the committee.

There are many people interested in the concept of virtual testing who have many questions and others who have been in the early adoption phase who have experiences that they could share. Virtual testing can be applied to digital, analog, mixed-signal and other testing for which the unit under test and the test apparatus can be represented by simulation.

The purpose of this TAC will be to help facilitate the development and adoption of virtual testing technologies and methodologies. It will bring together researchers, developers and users of virtual testing to provide a forum to foster exchange, discussion and development of ideas, research, requirements, issues and real experiences.

Ed Perkins, Integrated Measurement Systems



TTTC Standards News

STIL is Accepted by the IEEE-SA

At the March 1999 meeting of RevCom (the IEEE Standards Board Review Committee responsible for approval of all new standards efforts), the STIL effort was approved as a new standard, and is now officially known as IEEE Std. 1450-1999. Congratulations to all involved with making this effort a reality!

IEEE Std. 1450-1999 defines the Standard Test Interface Language (STIL) for Digital Test Vectors, facilitating the transportation of test vectors from Computer-Aided Engineering (CAE) environments to their application on Automated Test Equipment (ATE).

The STIL Working Group wants to explicitly thank all the members of the TTTC for supporting us - both directly and as the sponsor of this work.

Of course, there are still some final steps in the standards process before copies of the document are available. The official document is deep in the editorial review process, but all technical hurdles have been vaulted and now we're just checking the format. Current expectations are that the editorial process will end and the document will be in printing by the end of July or middle of August, 1999.

The acceptance of IEEE Std. 1450-1999 by the IEEE Standards Association is just the start of the STIL effort, as indicated in the related article.

For more information about STIL, please contact Greg Maston at g.a.maston@ieee.org, or visit our website, <http://grouper.ieee.org/groups/1450/>.

Greg Maston, Former Co-Chair of 1450



STIL Effort Expands with a New Series of PARs

With the acceptance of IEEE Std. 1450-1999 (STIL, or as the Working Group is now calling it, "dot-zero"), the path has been cleared for starting new efforts on a series of "dotted extension" PARs to STIL.

A PAR (Project Authorization Request) is the first step towards defining a new standard under the IEEE process. "Dotted Extension" PARs are defined to be extensions to original work.

The PARs for STIL Extensions were submitted to the IEEE following the approval of STIL. All of these efforts continue to be sponsored by the TTTC.

The following PARs have been approved by the IEEE as official projects:

- P1450.1: Extensions to STIL for Semiconductor Design Environments
- P1450.2: Extensions to STIL for DC Level Specification
- P1450.3: Extensions to STIL for Tester Target Specification
- P1450.4: Extensions to STIL for Test Flow Specification
- P1450.5: Extensions to STIL for Semiconductor Test Method Specification.

Each of these efforts has some initial definition behind it (it was impossible to have the Working Group sit still during STIL ballot recirculations). But there is a long path from concept to a document ready for balloting, and the Working Group - or, as it stands now, the five new Working Groups - are always open to additional volunteers.

The P1450.1 effort (Extensions for Design Environments) includes the constructs identified by the P1500 Task Force to support the Core Test Language (CTL). This is very much a joint effort between the STIL Working Group and the P1500 CTL Task Force. More details about this joint effort can be found on the P1500 website, at <http://grouper.ieee.org/groups/1500/>, as well as on the 1450 website.

A panel session is scheduled at ITC 99 to discuss the evolution of STIL.

Anyone with an interest in these efforts can contact Greg Maston, g.a.maston@ieee.org, or Tony Taylor, t.taylor@ieee.org, or visit the STIL website which contains more information about each of these efforts, at <http://grouper.ieee.org/groups/1450/>.

Greg Maston, Former Co-Chair of 1450.

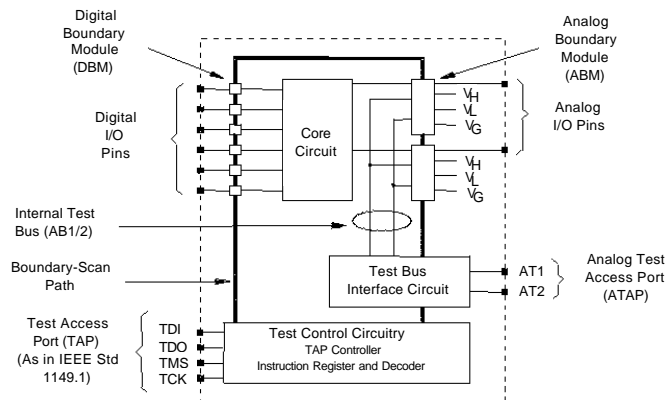


IEEE 1149.4 Working Group

The IEEE 1149.4 Standard for a Mixed-Signal Test Bus has reached a new milestone. On June 26, 1999, the IEEE-SA Standards Board approved the new Standard. This is great news for the Working Group, many of whom have been striving for this accomplishment together for nearly eight years. The new Standard will open up a whole new means of testing for mixed-signal systems. 1149.4 is the latest in a series of Standards sponsored by the TTTC.

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IEEE 1149.4 provides a means to funnel an analog stimulus and response to and from the system being tested. This analog measurement capability is delivered through devices compliant with the Standard via a virtual analog switching matrix under the control of the IEEE 1149.1 compatible boundary-scan data register. Each analog pin of a mixed-signal component compliant with the Standard will be able to source an analog current from, and deliver a voltage response to the Analog Test Bus.



As shown in the figure, above, each analog pin will also be able to emulate the digital action of the IEEE 1149.1 Standard: that of driving a static "high" and "low" voltage, and capturing a digitized response.

The next meeting of the IEEE 1149.4 Working Group will be held Friday October 1, from 8:00 AM to 6:00 PM at ITC 99 in Atlantic City. The location is yet to be determined. This year's ITC meeting will celebrate the promulgation of the Standard, see the election of new Working Group officers, begin the building of new BSDL constructs, and raise any issues going forward with the new Standard. As always, anyone with an interest is invited to attend this or any other IEEE meeting. For more information, please see the web page: <http://grouper.ieee.org/groups/1149/4/>.

Adam Cron, IEEE 1149.4 Working Group Chair



Miscellaneous

Book Review

"Random Testing of Digital Circuits: Theory and Applications" René David, Marcel Dekker, Inc., 1998
ISBN 0-8247-0182-8

The area of digital circuit testing is a key area in the electronics product development process. Random testing is finding more and more applications as complex digital devices are being developed and especially as Built-In Self Test (BIST) is increasingly finding its way in real products, both for production and lifetime testing. Concurrently, product quality requirements become more stringent, which requires a high degree of expertise in

specifying and assessing the quality of random testing. The book by René David is a key contribution to this field, coming from a worldwide recognized expert in the area for more than two decades.

Several excellent books have been previously written on random testing, but this book is distinctive. In part, the uniqueness of the book is associated with the two stated goals: first, starting with the fundamentals of digital testing, it guides the reader to reach an accurate understanding of random testing. Second, it achieves this using a didactic approach, with many easy to understand examples and figures and cross-references. I would say that there is a deep concern throughout the book, not only to introduce sound theory to quantify the conclusions and results, but also to assist the reader in understanding why these results are to be expected, and what factors can be used to improve them.

The text is written in such a way that different levels of reading and study can be pursued from a general overview of random testing and its main results to a detailed, deep study of this scientific discipline. Methods and tools are introduced with a clear statement of their domain of validity and, whenever feasible, the possibility of their extension to other domains is highlighted. This can be seen, for instance, in random testing of sequential circuits (chapter 7), which mainly deals with synchronous circuits, but also briefly addresses asynchronous circuits. Again, the topic is further explored in Appendix F.

These characteristics help us to identify the target audience of the book, which is not clearly stated in the Preface. The book may very well be used as a textbook for undergraduate or graduate course on digital design and test (I believe the two disciplines, design and test, should not be learned separately), and as a solid foundation for advanced research on random testing. However, the book includes many industrial applications, and can rewardingly be used by practitioners, like design and test engineers, as end users of the methods and tools described in the book. If it is to be used as a textbook, it would be rewarding to have suggestions on how to organize one or two-semester courses, or short courses. It would be also valuable to make available some additional material, like public domain software tools implementing some of the described algorithms, and the electronic version of slides of the figures included in it.

The book is organized in three parts and 13 chapters. In Part I (chapters 1, 2, 3 and 4), the basic principles and concepts of random testing are introduced, namely digital testing, BIST, fault models, functional and structural testing, test pattern generation and test quality assessment (referred to as "performance measurements") of a given test sequence.

Part II is devoted to the explanation of the basic principles of random testing for combinational and sequential circuits. This includes the underlying philosophy of random testing and the evaluation of the required test length for a circuit and a specified level of confidence in the test result, namely for sequential

circuits, RAMs and microprocessors.

Part III deals with the main aspects of random testing implementation. First, test generation is analyzed (chapters 10 and 11) and then signature analysis (chapter 12) and design for random testability (chapter 13) is addressed.

Finally, the book has an extensive Postface section with 13 appendices dealing with topics not addressed in the main body, plus a large collection of exercises (with solutions), illustrating the contents of all chapters and a thorough bibliography for further research. Each chapter ends with a Notes and References section.

In summary, René David presents a broad spectrum of topics on random testing of digital circuits at a level accessible to undergraduate students, and yet challenging for advanced graduate students and engineers working in industry. The book is well written, readable, reliable and accurate. It is a gem. It should be on the shelf (and not only there!) of all professionals dealing with digital testing.

*Reviewed by J. Paulo Teixeira IST, Lisbon Technical University / INESC
December, 1998*



Nominations for TTTC Chair or Vice Chair

In accordance with the bylaws, TTTC will elect a Chair and two Vice-Chairs for 2000-2001. Nominations for candidates for these offices are made either by the TTTC Nominations Committee or by petition from the members.

As a member, you have two choices if you wish to have someone nominated:

1. You can propose a nominee to the Nominations Committee, who can either accept or dismiss their proposal, or
2. You can nominate by petition.

To propose a nominee to the Nominations Committee, contact the Committee Chair: Fred Liguori, Tel: +1-609-893-5140, E-mail: ffliguori@aol.com.

As posted on the TTTC web site, to nominate a candidate by petition, circulate a petition to TTTC members with the name and a short biography (career and TTTC contribution history) of the person you propose as a candidate. All nominees must be full members of TTTC. Petitions must be signed by 10 or more current TTTC members who are IEEE members. Petition signatures must be accompanied by valid IEEE member numbers. Send petition nominations with petitioned candidate's biography and statement by August 23rd to the TTTC Office, 1474 Freeman Dr., Amissville, VA 20106, USA.

Fred Liguori, TTTC Nominations Committee Chair



Award Recommendations Solicited

Each year, TTTC recognizes members for their outstanding service by presenting service awards through the Award Program of the IEEE Computer Society. These service awards, which are presented during TTTC-sponsored events, but principally during the Awards Banquet of ITC Test Week, generally fall in one of the four following categories:

Certificate of Appreciation: for creditable service to any TTTC activity or program.

Meritorious Service Award: for meritorious and significant service to any TTTC activity or program (qualification is enhanced by the level and number of contributions, excellence, dedication and tenure of service).

Distinguished Service Award: for long and distinguished service to the TTTC at a level of dedication and achievement rarely demonstrated.

Outstanding Contribution Certificate: for an achievement of major value and significance to TTTC (the achievement should be a specific, concisely characterized accomplishment, as opposed to a collection of different efforts).

If you know someone who should be recognized during the next ITC Test Week (October 18-23, 1999), or if you would like to learn more about TTTC awards, please contact the TTTC Awards Chair, Christian Landraul, Tel: +33-67-41-85-24, Fax: +33-67-41-85-00, E-mail: landraul@lirmm.fr.

Christian Landraul, TTTC Awards Chair



TTTC Consolidated Database Project

After many years of dedicated work on the part of the TTTC volunteers, a great amount of data concerning TTTC members, TTTC co-sponsored events, Awards, Standards, Technical Activity Committees, etc. has been collected. Unfortunately, until now, all this valuable data was distributed in many databases, without a common data structure or user interface, and with many inconsistent redundancies. Obviously such a huge amount of information should not only be saved, but also made profitably and efficiently usable.

To pursue this mission, the TTTC Communications decided to start the TTTC Consolidated Database Project with the primary target of setting up, within 6 months, a unique repository of information items about TTTC members, TTTC events, TTTC Awards and other useful

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data. As a secondary goal, the project will define a strategy to make part of the data accessible through the Web to selected groups of users (e.g., General chairs, TACs Chairs, Group Chairs, ...) according to predefined and differentiated privileges.

In order to build a database which meets the needs of the TTTC officers' community as closely as possible, the TTTC Database Group is currently collecting a set of user requirements that will allow, by the end of July, definition of the final database specifications in terms of data structures and basic services. The structure will be later normalized and eventually implemented utilizing Microsoft Access.

Alfredo Benso, Ph.D., TTTC Consolidated Database Project Co-Chair



IEEE Design & Test of Computers

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- March 15, 2000: Authors notified of acceptance with requested revisions
- July 25, 2000: Final copy due to Design & Test Managing Editor
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